What is Claimed is:

1. A method of accessing a memory device using a plurality of user-defined commands, comprising:

(a) providing a set of commands for controlling access to the memory device, wherein the set of commands includes the plurality of user-defined commands;

(b) storing in the memory device a set of memory access parameters associated with each user-defined command, wherein each set of memory access parameters includes at least one memory access parameter; and

(c) accessing the memory device using the user-defined commands, wherein each memory access commanded by a user-defined command is controlled in accordance with the set of memory access parameters associated with the user-defined command.

2. The method of claim 1, wherein the memory access parameters include a burst length.

3. The method of claim 1, wherein the memory access parameters include at least one of a read latency and a write latency.

4. The method of claim 1, wherein the set of commands further includes a program command for programming the user-defined commands into the memory device.

5. The method of claim 4, further comprising:

(d) identifying from an operational code a user-defined command to be programmed in response to receiving the program command.

6. The method of claim 5, wherein (b) further includes:

storing in the memory device a command definition associated with the user-defined command identified from the operational code, wherein the command definition includes a memory access command and the set of memory access parameters.

7. The method of claim 6, wherein the memory access command is one of: a read command, a write command, and a terminate command.

8. The method of claim 6, wherein the set of memory access parameters includes a burst length and at least one of a read latency and a write latency.

9. The method of claim 5, wherein the operational code associated with the program command is received by the memory device via an address bus.

10. The method of claim 5, wherein the operational code associated with the program command is received via a data bus.

11. The method of claim 4, further comprising:

(d) identifying from an operational code a non-programmable command to be executed in response to receiving the program command.

12. The method of claim 11, wherein the non-programmable command is one of: an auto refresh command, a mode register set command, a no operation command, and a drive strength setting command.

13. A method of programming a memory device to support a plurality of user-defined commands, comprising:

sending a program command from a controller to the memory device, wherein the program command indicates that a user-defined command is to be programmed in the memory device;

sending an operational code associated with the program command from the controller to the memory device, wherein the operational code indicates which of the plurality of user-defined commands is to be programmed;

sending a command definition from the controller to the memory device, wherein the command definition includes a memory access command and at least one memory access parameter; and

storing the command definition in the memory device such that the command definition is associated with the user-defined defined command indicated by the operational code.

14. The method of claim 13, wherein the memory access command is one of a read

command, a write command, and a terminate command.

15. The method of claim 13, wherein the at least one memory access parameter includes a burst length.

16. The method of claim 13, wherein the least one memory access parameter includes at least one of a read latency and a write latency.

17. A method of accessing a memory device using a plurality of user-defined commands, comprising:

(a) providing a set of commands for controlling access to the memory device, wherein the set of commands includes the plurality of user-defined commands and a program command for programming the user-defined commands into the memory device;

(b) programming the user-defined commands by storing command definitions associated with the user-defined commands in the memory device in response to receipt of program commands, wherein each of the command definitions comprises a memory access command and a set of memory access parameters including a burst length and at least one of a read latency and a write latency; and

(c) accessing the memory device using the user-defined commands, wherein each memory access commanded by a user-defined command is controlled in accordance with the set of memory access parameters associated with the user-defined command.

18. The method of claim 17, further comprising:

(d) sending with each program command an operational code, wherein the operational code includes a first set of bits that indicate which, if any, of the user-defined commands is to be programmed via the command definition and a second set of bits that indicate which, if any, of a set of non-programmable commands is to be executed.

19. The method of claim 18, wherein the set of non-programmable commands includes at least one of: an auto refresh command, a mode register set command, a no operation command, and a drive strength setting command.

20. A method of accessing a memory device, comprising:

(a) providing a set of commands for controlling access to the memory device, wherein the set of commands includes a plurality of user-defined commands that are programmable in the memory device and at least one additional command for controlling the memory device with a non-programmable command;

(b) accessing the memory device using the user-defined commands, wherein each memory access commanded by a user-defined command is controlled in accordance with a set of memory access parameters associated with the user-defined command; and

(c) executing a non-programmable command in response to receipt of the at least one additional command, wherein the non-programmable command is specified in an operational code received in connection with the at least one additional command.

21. The method of claim 20, wherein the non-programmable command is one of: an auto refresh command, a mode register set command, a no operation command, and a drive strength setting command.

22. A memory device controllable with user-defined commands, comprising:

a memory array accessible for reading and writing data therein;

a command module that receives commands for controlling access to the memory array, wherein a set of commands for controlling access to the memory array includes a plurality of user-defined commands; and

a mode module that stores command definitions respectively associated with the user-defined commands, wherein each command definition includes a memory access command and at least one memory access parameter, and wherein each memory array access commanded by a user-defined command is controlled in accordance with the at least one memory access parameter in the command definition associated with the user-defined command.

23. The memory device of claim 22, wherein the memory access command is one of a read command, a write command, and a terminate command.

24. The method device of claim 22, wherein the at least one memory access parameter includes a burst length.

25. The memory device of claim 22, wherein the least one memory access parameter includes at least one of a read latency and a write latency.

26. The memory device of claim 22, wherein the set of commands further includes a program command for programming the user-defined commands into the mode module, and wherein the command module commands the mode module to program a user-defined command in response to receipt of the program command.

27. The memory device of claim 26, wherein the command module commands the mode module to program a user-defined command specified by an operational code received in connection with the program command.

28. The memory device of claim 27, wherein the operational code is received by the command module via an address bus.

29. The memory device of claim 27, wherein the operational code is received by the command module via a data bus.

30. The memory device of claim 22, wherein the set of commands further includes an additional command for controlling the memory device with a non-programmable command.

31. The memory device of claim 30, wherein the non-programmable command is specified in an operational code received by the command module in connection with the additional command.

32. The memory device of claim 30, wherein the non-programmable command is one of: an auto refresh command, a mode register set command, a no operation command, and a drive strength setting command.

33. The memory device of claim 22, further comprising:

a memory array control module coupled to the memory array, that receives memory access commands from the mode module in response to receipt of a user-defined command,

wherein the memory array control module controls access to the memory array in accordance with the memory access parameters associated with the user-defined command.

34. The memory device of claim 33, further comprising:

an address latch/counter module that receives an input address associated with a user-defined command and supplies addresses to the memory array control module during memory access in accordance with the memory access parameters associated with the user-defined command.

35. The memory device of claim 22, wherein the memory device is a dynamic random access memory (DRAM).

36. A memory device controllable with user-defined commands, comprising:

means for storing data that is accessible for reading and writing data therein;

means for processing input commands for controlling access to the means for storing data, wherein a set of commands for controlling access to the means for storing data includes a plurality of user-defined commands; and

means for storing command definitions respectively associated with the user-defined commands, wherein each command definition includes a memory access command and at least one memory access parameter, and wherein each memory array access commanded by a user-defined command is controlled in accordance with the at least one memory access parameter in the command definition associated with the user-defined command.

37. The memory device of claim 36, wherein the memory access command is one of a read command, a write command, and a terminate command.

38. The memory device of claim 36, wherein the at least one memory access parameter includes a burst length.

39. The memory device of claim 36, wherein the least one memory access parameter includes at least one of a read latency and a write latency.

40. The memory device of claim 36, wherein the set of commands further includes a

program command for programming the user-defined commands into the means for storing command definitions, and wherein the means for processing input commands commands the means for storing command definitions to program a user-defined command in response to receipt of the program command.

41. The memory device of claim 40, wherein the means for processing input commands commands the means for storing command definitions to program a user-defined command specified by an operational code received in connection with the program command.

42. The memory device of claim 41, wherein the operational code is received by the means for processing input commands via an address bus.

43. The memory device of claim 41, wherein the operational code is received by the means for processing input commands via a data bus.

44. The memory device of claim 36, wherein the set of commands further includes an additional command for controlling the memory device with a non-programmable command.

45. The memory device of claim 44, wherein the non-programmable command is specified in an operational code received by the means for processing input commands in connection with the additional command.

46. The memory device of claim 44, wherein the non-programmable command is one of: an auto refresh command, a mode register set command, a no operation command, and a drive strength setting command.

47. The memory device of claim 36, further comprising:

means for controlling the means for storing data that receives memory access commands from the means for storing command definitions in response to receipt of a user-defined command, wherein the means for controlling the means for storing data controls access to the means for storing data in accordance with the memory access parameters associated with the user-defined command.

48. The memory device of claim 36, wherein the memory device is a dynamic random access memory (DRAM).

49. A controller for controlling a memory device, comprising:

a memory management module that manages access to the memory device; and

a command generator module that generates commands for accessing the memory module in accordance with the memory management module, wherein the commands include a plurality of user-defined commands and a program command for programming the user-defined commands into the memory device, and wherein the controller sends to the memory device a command definition associated with a user-defined command to be programmed, the command definition including a memory access command and at least one memory access parameter.

50. The controller of claim 49, wherein the controller sends to the memory device an operational code indicating which user-defined command is to be programmed in connection with a program command.

51. The controller of claim 49, wherein the memory access command is one of a read command, a write command, and a terminate command.

52. The controller of claim 49, wherein the at least one memory access parameter includes a burst length.

53. The controller of claim 49, wherein the least one memory access parameter includes at least one of a read latency and a write latency.